IN THE CLAIMS:

Please amend the claims as set forth below in marked-up form. In accordance with current amendment practice, a clean copy of the claims has been omitted.

1. (Currently Amended) A nonvolatile semiconductor memory device comprising a plurality of memory elements formed in the vicinity of the surface of a substrate, a plurality of word lines for driving the memory elements, and a plurality of bit lines,

each of said plurality of memory elements including:

a semiconductor channel forming region formed in the vicinity of the surface of the substrate,

a source region in contact with the channel forming region in the vicinity of the surface of the substrate,

a drain region in contact with the channel forming region at a position facing the source region in the vicinity of the surface of the substrate,

a gate insulating film, including a tunnel insulating film, formed on said substrate adjacent to the channel forming region,

a top insulating film formed on said gate insulating film;

a conductive gate electrode formed on the top insulating film on the gate insulating film, and

a charge storing means facing said surface of the channel forming region and which is provided in the tunnel insulating film and in the gate insulating film and is planarly dispersed to the other neighbor charge storing means in the gate insulating film;

the gate electrode of the plurality of memory elements being respectively connected to the plurality of word lines;

wherein said gate insulating film formed adjacent to the semiconductor channel forming region comprises a Fowler-Nordheim

(FN) type tunneling film which has a FN type tunneling electroconductivity, said FN type tunneling film being made entirely of material having a dielectric constant greater than that of silicon oxide and formed so as to be in direct contact with said channel forming region.

2. (Previously Presented) The nonvolatile semiconductor memory device according to claim 1, wherein the FN type tunneling film comprises any one of a nitride film, an oxynitride film, and aluminum oxide film, a tantalum pentaoxide film and a BST ($BaSrTiO_3$) film, having an FN tunneling electroconductivity.

3. (Withdrawn) A nonvolatile semiconductor memory device according to claim 1, wherein the gate insulating film includes a buffer layer formed between the FN type tunneling film and the channel forming region and suppressing an interface trap level.

4. (Currently Amended) The nonvolatile semiconductor memory device according to claim 1, wherein the gate insulating film comprises a Pool-Frenkel (PF) type film including any one of a nitride film, an oxynitride film, ~~and~~an aluminum oxide film, a tantalum pentaoxide film and a BST ($BaSrTio_3$) film, having a ~~FN~~ PF type electroconductivity.

5. (Withdrawn) A nonvolatile semiconductor memory device according to claim 4, wherein the gate insulating film includes a buffer layer formed between the FN type tunneling film and the PN film.

6. (Previously Presented) The nonvolatile semiconductor memory device according to claim 1, further comprising:

a pull-up electrode in the vicinity of the gate electrode or a wiring layer connected to the gate electrode, via a dielectric film; and

a pull-up gate bias means for applying a voltage to the pull-up electrode.

7. (Previously Presented) The nonvolatile semiconductor memory device according to claim 6, wherein

a plurality of gate electrodes of the plurality of memory transistors are connected to a plurality of word lines, and

a selected transistor is connected between the pull-up gate bias means and the pull-up electrode, said pull-up gate bias means supplying a voltage having a polarity the same as a polarity of a boosting voltage for boosting the precharged word line by a capacitance coupling.

8. (Previously Presented) The nonvolatile semiconductor memory device according to claim 6, wherein the pull-up electrode is arranged in the vicinity of an upper portion of the gate electrode or a connection layer connected to the gate electrode, via the dielectric film.

9. (Previously Presented) The nonvolatile semiconductor memory device according to claim 1, wherein each memory transistor comprises said source region contacted to the channel forming region, and said drain region spaced to the source region and contacted to the channel forming region,

wherein a plurality of gate electrodes of the plurality of memory transistors are connected to a plurality of word lines,

wherein the source region and drain region of each memory transistor are connected to a common line in a bit line direction, electrically insulated to and intersecting the word line, and

wherein said nonvolatile semiconductor memory device further comprises

a write inhibit voltage supply means for supplying a reverse-biased voltage to the source region and/or the drain region of the memory transistor the gate electrode of which is connected to the word line selected at a writing, through the common line, to make the source region and/or the drain region in a reverse-biased state to the channel forming region, and

a non-selected word line biasing means for supplying a voltage to a non-selected word line at the writing, a polarity of the voltage being a polarity making the non-selected word line in a reverse biased state to the channel forming region.

10. (Previously Presented) The nonvolatile semiconductor memory device according to claim 9, wherein the write inhibit voltage supply means supplies the reverse bias voltage to the source region and/or the drain region to make a bias voltage of the memory transistor connected to the selected word line to thereby prevent an erroneous write and/or an erroneous erase.

11. (Previously Presented) The nonvolatile semiconductor memory device according to claim 9, wherein the non-selected word line biasing means supplies a voltage having a polarity for reverse-biasing to the non-selected word line to make a bias voltage or the memory transistor connected to the non-selected word line to thereby prevent an erroneous write and/or an erroneous erase.

12. (Previously Presented) The nonvolatile semiconductor memory device according to claim 9, wherein the non-selected word line biasing means biases the gate electrode to the source region so that a voltage of the gate electrode becomes a low level equal or lower than an inhibit gate voltage.

Claims 13 to 51. (Cancelled)

52. (Withdrawn) A nonvolatile memory device according to claim 1 wherein said gate insulating film includes a buffer layer adjacent said tunnel insulating film and said surface of the substrate.

53. (Previously Presented) The nonvolatile semiconductor memory device according to claim 1 wherein said gate insulating film includes a tunnel insulating film, a nitride film, and said top insulating film in that order sandwiched between said surface of said substrate and said gate electrode, a portion of said gate insulating film overlapping each of said source region and said drain region.

54. (Previously Presented) A nonvolatile semiconductor memory device comprising a plurality of memory elements formed in the vicinity of the surface of a substrate, a plurality of word lines for driving the memory elements, and a plurality of bit lines;

each of said plurality of memory elements including:

a semiconductor channel forming region formed in the vicinity of the surface of the substrate;

a source region in contact with the channel forming region in the vicinity of the surface of the substrate;

a drain region in contact with the channel forming region at a position facing the source region in the vicinity of the surface of the substrate;

a gate insulating film, including a tunnel insulating film, formed on said substrate adjacent to the channel forming region;

a top insulating film formed on said gate insulating film;

a conductive gate electrode formed on the top insulating film on the gate insulating film;

a charge storing means facing said surface of the channel forming region and which is provided in the tunnel insulating film and in the gate insulating film and is planarly dispersed to the other neighbor charge storing means in the gate insulating film;

a pull-up electrode in the vicinity of the gate electrode or a wiring layer connected to the gate electrode, via a dielectric film; and

a pull-up gate bias means for applying a voltage to the pull-up electrode;

the gate electrode of the plurality of memory elements being respectively connected to the plurality of word lines;

wherein said gate insulating film formed adjacent to the semiconductor channel forming region comprises a Fowler-Nordheim (FN) type tunneling film which has a FN type tunneling electroconductivity and contains material having a dielectric constant greater than that of silicon oxide.

55. (Previously Presented) The nonvolatile semiconductor memory device according to claim 54, wherein

a plurality of gate electrodes of the plurality of memory transistors are connected to a plurality of word lines; and

a selected transistor is connected between the pull-up gate bias means and the pull-up electrode, said pull-up gate bias

means supplying a voltage having a polarity the same as a polarity of a boosting voltage for boosting the precharged word line by a capacitance coupling.

56. (Previously Presented) The nonvolatile semiconductor memory device according to claim 54, wherein the pull-up electrode is arranged in the vicinity of an upper portion of the gate electrode or a connection layer connected to the gate electrode, via the dielectric film.

57. (Previously Presented) The nonvolatile semiconductor memory device according to claim 9, wherein when the reverse bias voltage is supplied to the channel forming region while the gate electrode and the channel forming region of the memory transistor are kept at a same potential level, depletion layers extend from the source region and drain region to the channel forming region to merge them.

58. (Previously Presented) The nonvolatile semiconductor memory device according to claim 9, wherein the gate length of the memory transistor is shorter than a gate length given by, when the reverse bias voltage is supplied while the gate electrode and the channel forming region are kept at a same potential level, merged depletion layers extended from the source region and the drain region to the channel forming region.

59. (Previously Presented) The nonvolatile semiconductor memory device according to claim 1, wherein each memory transistor comprises:

a source region contacted to the channel forming region; and

a drain region spaced to the source region and contacted to the channel forming region;

wherein said nonvolatile semiconductor memory device comprises:

a source line commonly connecting the plurality of source regions of the plurality of memory transistors in the bit line direction; and

a word line commonly connecting the plurality of gate electrodes of the plurality of memory transistors in a word direction.

60. (Previously Presented) The nonvolatile semiconductor memory device according to claim 1, wherein each memory transistor comprises:

a source region contacted to the channel forming region; and

a drain region spaced to the source region and contacted to the channel forming region;

wherein said nonvolatile semiconductor memory device comprises:

sub source lines commonly connecting the plurality of source regions of the plurality of memory transistors in a bit line direction;

a main source line commonly connecting the sub source lines in the bit line direction;

sub bit lines commonly connecting the plurality of drain regions of the plurality of memory transistors in the bit line direction;

a main bit line commonly connecting the sub bit line in the bit line direction;

a word line commonly connecting the plurality of gate electrodes of the plurality of memory transistors in a word direction; and

a selected memory transistor being connected between the sub source line and the main source line and between the sub bit line and the main bit line.

61. (Previously Presented) The nonvolatile semiconductor device according to claim 1, wherein the plurality of memory transistors are connected in series between a first selected transistor connected to a bit line and a second selected transistor connected to a common potential line.

62. (Withdrawn) The nonvolatile semiconductor memory device according to claim 1, wherein each memory transistor comprises a source region contacted to the channel forming region, and a drain region spaced to the source region and contacted to the channel forming region,

wherein said nonvolatile semiconductor memory device comprises:

a plurality of element separation regions for isolating the respective memory transistors by insulation;

a common line commonly connecting the source regions or the drain regions in a bit line direction; and

a word line connecting the plurality of gate electrodes in a word direction;

wherein the plurality of element separation regions are formed as lines along the bit line direction and spaced from each other; and

wherein the common line intersects and is electrically isolated to the word line, is connected to one of the source region or the drain region, and is wired on the element

separation regions by avoiding a wiring passing on another region of the source region or the drain region which is not connected to the common line.

63. (Withdrawn) The nonvolatile semiconductor memory device according to claim 62, wherein the plurality of element separation regions are formed as parallel strips having a width approximately equal to that of the rod line, adjacent strips being spaced as adjacent word lines;

wherein a self-aligned contact hole is formed on the source region and the drain region by using a sidewall insulation layer formed on sidewalls of the word line; and

wherein the common line wired on the element separation regions is commonly connected to the one region through the self-aligned contact hole and is wired by a winding manner in the bit line direction.

64. (Previously Presented) The nonvolatile semiconductor memory device according to claim 1, wherein the charge storing means does not have conductivity as a whole facing to the channel forming region when charges are not moved to the outside of the memory transistor.

65. (Withdrawn) The nonvolatile semiconductor memory device according to claim 64, wherein the gate insulating film comprises:

a tunneling insulating film formed on the channel forming region; and

a nitride film or an oxide nitride film, formed on the tunneling insulating film.

66. (Withdrawn) The nonvolatile semiconductor memory device according to claim 64, wherein the gate insulating film comprises:

a tunneling insulating film formed on the channel forming region; and

conductors, including small sized conductive material, formed on the tunneling insulating film as the charge storing means and isolated from each other.